

ALLAMA IQBAL OPEN UNIVERSITY, ISLAMABAD
(Department of Computer Science)

WARNING

1. **PLAGIARISM OR HIRING OF GHOST WRITER(S) FOR SOLVING THE ASSIGNMENT(S) WILL DEBAR THE STUDENT FROM AWARD OF DEGREE/CERTIFICATE, IF FOUND AT ANY STAGE.**
2. **SUBMITTING ASSIGNMENTS BORROWED OR STOLEN FROM “AIOU PLAGIARISM POLICY”.**

Course: Digital Logic Design (3409)
Level: Bachelor

Semester: Autumn, 2013
Total Marks: 100

ASSIGNMENT No. 1

Note: All questions carry equal marks.

- Q. 1 Add and multiply the following numbers in the given base without converting to decimal:
- (a) $(1203)_4$ and $(332)_4$
 - (b) $(612.3)_8$ and $(62.6)_8$
 - (c) $(297)_{12}$ and $(128)_{12}$
- Q. 2 Demonstrate by means of truth tables the proof of De Morgan's Laws for three variables and distributive law of * over +.
- Q. 3 Given the Boolean function: $F = xyz + xy'z' + y'z$ implement it with:
- (a) AND, OR, and NOT Gates
 - (b) Only OR and Not Gates
 - (c) Only AND and NOT Gates
- Q. 4 a) Obtain the simplified expressions in sum of products for the following Boolean Function:
 $x'z + w'xy' + w(x'y + xy')$
- b) Simplify the Boolean function F using the don't-care condition d, in (1) sum of products and (2) product of sums:
 $F = ACE + A'CD'E' + A'C'DE, d = DE' + A'D'E + AD'E'$
- Q. 5 a) Obtain the NAND logic diagram of a full-adder from the Boolean function:
 $C = xy + xz + yz$ and $S = C' (x + y + z) + xyz$

- b) Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number.

ASSIGNMENT No. 2

Total Marks: 100

Note: All questions carry equal marks.

- Q. 1 Design an excess-3-to-BCD code converter using a 4-bit full-adders MSI circuit.
- Q. 2 Using MSI circuits, construct a binary parallel adder to add two 16-bit binary number and label all carries between the MSI circuits.
- Q. 3 Draw the logic diagram (showing all gates) of a master-slave D flip-flop. Using NAND gates.
- Q. 4 a) Design a BCD counter with JK flip-flops.
b) What is the difference between serial and parallel transfer? What type of register is used in each case?
- Q. 5 a) Draw the interconnection of I²L gates to form a 2 * 4 decoder.
b) Calculate the noise margin of the ECL gate.

3409 Digital Logic Design

Credit Hours: 4 (4+0)

Recommended Book: Digital Logic Design by Morris Mano

Course Outlines:

- Unit-1: Binary System**
Binary Numbers Based Conversion of Octal, Hexadecimal and Binary, Complements, Binary Codes, Binary Logic and ICs
- Unit-2: Boolean Algebra and Logic Gates**
Definitions, Theorems and Properties, Boolean Functions, Canonical and STD Forms, other Logical Properties, Gates
- Unit-3: Simplification of Boolean Function**
Map Method, NAND and NOR Implementation, Tabulation Method, Prime Implement
- Unit-4: Combination Logic**
Design Procedure, Adder, Subtractors, Code Conversation Analysis Procedure, NAND and NOR Functions, Ex-OR and Ex-NOR Function
- Unit-5: Combination Logic with MSI and LSI**
Binary Parallel Adder, Decimal Adder, BCD Counter, Magnitude Compactor, Decoders, Demultiplexers, Encoder, Multiplexer, ROM, PLA
- Unit-6: Sequential Logic**
Introduction, Flip Flop, Triggering, State Reduction Excitation Table, Design Procedure, Design of Counter
- Unit-7: Register, Counter, and Memory Unit**
Register Counter, Timing Sequence, Memory Unit
- Unit-8: Asynchronous Sequential Logic**
Analysis Procedure, Circuits with Latches, Design Procedure, Reductions of State and Flow Tables, Race Free State Assignment
- Unit-9: Digital Integrated Circuits**
Bipolar Transistor Characteristics, RTL and DTL Circuits, Transistor, Transistor Logic, Emitter Coupled Logic (ECL), Metal Oxide Semiconductor (MOS), CMOS